



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/705,668	11/02/2000	Darrell D. Boggs	042390.P9576	6260

7590 11/26/2004
Eric S Hyman
Blakely Sokoloff Taylor & Zafman LLP
12400 Wilshire Boulevard
7th Floor
Los Angeles, CA 90025

EXAMINER

LI, AIMEE J

ART UNIT PAPER NUMBER

2183

DATE MAILED: 11/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/705,668

Applicant(s)

BOGGS ET AL.

Examiner

Aimee J Li

Art Unit

2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 September 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 and 11-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 and 11-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|-----------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input checked="" type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. <u>11/17/04</u> . |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-9 and 11-24 have been considered. Claim 10 has been cancelled as per Applicant's request.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

3. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

4. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-9 and 12-21 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-19 of copending Application No. 09/705,678. Although the conflicting claims are not identical, they are not patentably distinct from each other because all the limitations in the above claims are found within the copending applications claims.

6. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

7. Claims 1-19 of copending Application No. 09/705,678 contain every element of claims 1-9 and 12-21 of the instant application and as such anticipate claims 1-9 and 12-21 of the instant application. Please see below for a table mapping the claim limitations of the instant application with the copending application.

Copending Application 09/705,678	Instant Application 09/705,668
A replay queue to receive a plurality of instructions (Claim 1);	A replay queue to receive a plurality of instructions (Claim 1);
An execution unit to execute the plurality of instructions (Claim 1);	An execution unit to execute the plurality of instructions (Claim 1);
A scheduler coupled between the replay queue and the execution unit to speculatively schedule instructions for execution based on data dependencies and expected latencies of said plurality of instructions (Claim 1);	A scheduler coupled between the replay queue and the execution unit to speculatively schedule instructions for execution (Claim 1);
A counter to count a number of times an instruction has one of executed and replayed (Claim 1),	To increment a counter for each of the plurality of instructions to reflect the number of times each of the plurality of instructions has been executed (Claim 1);
Wherein independent instructions and associated dependent instructions are executed if the counter is less than a predetermined value and if the counter exceeds the predetermined value the instruction is prevented from executing until data required by the instruction is available (Claim 1);	To dispatch each instruction of the plurality of instructions to the execution unit either when the counter does not exceed a maximum number of replays or, if the counter for the instruction exceeds the maximum number of replays, when the instruction is safe to execute (Claim 1);
A checker coupled to the execution unit to	A checker coupled to the execution unit to

determine whether each instruction of the plurality of instructions has executed successfully, and coupled to the replay queue to dispatch to the replay queue each instruction that has not executed successfully (Claim 1).	determine whether each instruction has executed successfully, and couples to the replay queue to communicate to the replay queue each instruction that has not executed successfully (Claim 1).
An allocator/renamer coupled to the replay queue to allocate and rename those of a plurality of resources needed by the instruction (Claims 2 and 13).	An allocator/renamer coupled to the replay queue to allocate and rename those of a plurality of resources needed by the instruction (Claims 2 and 15)
A front end coupled to the allocator/renamer to provide the plurality of instructions to the allocator/renamer (Claims 3 and 14).	A front end coupled to the allocator/renamer to provide the plurality of instructions to the allocator/renamer (Claims 3 and 16).
A retire unit to retire the plurality of instructions, coupled to the checker to receive those of the plurality of instructions that have executed successfully, and coupled to the allocator/renamer to communicate a de-allocate signal to the allocator/renamer (Claims 4 and 15).	A retire unit to retire the plurality of instructions, coupled to the checker to receive those of the plurality of instructions that have executed successfully, and coupled to the allocator/renamer to communicate a de-allocate signal to the allocator/renamer (Claims 4 and 17).
Wherein the retire unit is further coupled to the replay queue to communicate a retire signal when one of the plurality of instructions is	Wherein the retire unit is further coupled to the replay queue to communicate a retire signal when one of the plurality of instructions is

retired such that the retired instruction and a plurality of associated data are removed from the replay queue (Claims 5 and 16).	retired (Claims 5 and 18).
At least one cache system on a die of the processor (Claim 6);	At least one cache system on a die of the processor (Claim 6);
A plurality of external memory devices (Claim 6); and	A plurality of external memory devices (Claim 6); and
A memory request controller coupled to the execution unit to obtain a plurality of data from the at least one cache system and the plurality of external memory devices and to provide the plurality of data to the execution unit (Claim 6).	A memory request controller coupled to the execution unit to obtain a plurality of data from the at least one cache system and the plurality of external memory devices (Claim 6).
Wherein the at least one cache system comprises a first level cache system and a second level cache system (Claim 7).	Wherein the at least one cache system comprises a first level cache system and a second level cache system (Claim 7).
Wherein the external memory devices comprise at least one of a third level cache system, a main memory, and a disk memory (Claim 8).	Wherein the external memory devices comprise at least one of a third level cache system, a main memory, and a disk memory (Claim 8).
A staging queue coupled between the checker and the scheduler (Claim 9).	A staging queue coupled between the checker and the scheduler (Claim 9).

Wherein the checker comprises a scoreboard to maintain a status of a plurality of resources (Claim 10).	Wherein the checker comprises a scoreboard to maintain a status of a plurality of resources (Claim 12).
A replay queue to receive a plurality of instructions (Claim 11);	A replay queue to receive a plurality of instructions (Claim 13);
At least two execution units to execute the plurality of instructions (Claim 11);	At least two execution units to execute the plurality of instructions (Claim 13);
At least two schedulers coupled between the replay queue and the execution units to schedule instructions for execution based on data dependencies and instruction latencies (Claim 11);	At least two schedulers coupled between the replay queue and the execution units to schedule instructions for execution (Claim 13);
A counter to count a number of times an instruction has one of executed and replayed (Claim 11);	To increment a counter for each of the plurality of instructions to reflect the number of times each of the plurality of instructions has been executed (Claim 13);
Wherein independent instructions and associated dependent instructions are executed if the counter is less than a predetermined value and if the counter exceeds the predetermined value the instruction is prevented from executing until data required	To dispatch each instruction of the plurality of instructions to the execution unit either when the counter does not exceed a maximum number of replays or, if the counter for the instruction exceeds the maximum number of replays, when the instruction is safe to execute

by the instruction is available (Claim 11);	(Claim 13);
A checker coupled to the execution unit to determine whether each instruction has executed successfully, and couples to the replay queue to communicate to the replay queue each instruction that has not executed successfully (Claim 11).	A checker coupled to the execution unit to determine whether each instruction has executed successfully, and couples to the replay queue to communicate to the replay queue each instruction that has not executed successfully (Claim 13).
A plurality of memory devices coupled to the execution units such that the checker determines whether the instruction has executed successfully based on a plurality of information provided by the memory devices (Claim 12).	A plurality of memory devices coupled to the execution units such that the checker determines whether the instruction has executed successfully based on a plurality of information provided by the memory devices (Claim 14).
Receiving an instruction of a plurality of instructions (Claim 17);	Receiving an instruction of a plurality of instructions (Claim 19);
Placing the instruction in a queue with other instructions of the plurality of instructions (Claim 17);	Placing the instruction in a queue with other instructions of the plurality of instructions (Claim 19);
Speculatively re-ordering those of the plurality of instructions in a scheduler based on data dependencies and instruction latencies (Claim 17);	Speculatively re-ordering those of the plurality of instructions in a scheduler based on data dependencies and instruction latencies (Claim 19);

Dispatching one of the plurality of instructions to an execution unit to be executed (Claim 17)	Dispatching one of the plurality of instructions to an execution unit to be executed (Claim 19)
Counting a number of times an instruction has one of executed and replayed, wherein the instruction and associated dependent instructions are executed if the number of times the instruction has one of executed and replayed is less than a predetermined value and if the number of times the instruction has one of executed and replayed exceeds the predetermined value the instruction is prevented from executing until data required by the instruction is available (Claim 17);	Either when a counter for the instruction does not exceed a maximum number of replays or, if the counter for the instruction exceed the maximum number of replays, when a required data for the instruction is available (Claim 19)
Executing the instruction (Claim 17);	Executing the instruction (Claim 19);
Determining whether the instruction executed successfully (Claim 17); and	Determining whether the instruction executed successfully (Claim 19); and
Routing the instruction and all associated dependent instructions back to the queue if the instruction did not execute successfully (Claim 17);	Routing the instruction back to the queue if the instruction did not execute successfully (Claim 19).
Retiring the instruction if the instruction executed successfully and allowing the	Retiring the instruction if the instruction executed successfully (Claim 19);

instruction's associated dependent instructions to execute (Claim 17),	
Allocating those of a plurality of system resources used by the instruction being retired (Claim 18).	Allocating those of a plurality of system resources used by the instruction being retired (Claim 20).
De-allocating those of the plurality of system resources used by the instruction being retired (Claim 18); and	De-allocating those of the plurality of system resources used by the instruction being retired (Claim 21); and
Removing the instruction and a plurality of related data from the queue (Claim 18).	Removing the instruction and a plurality of related data from the queue (Claim 21).

Response to Arguments

8. Examiner withdraws the drawing objections in favor of the Preliminary Amendment, now entered in the case.
9. Examiner withdraws the specification objections in favor of the amended specification.
10. Applicant's arguments filed 15 September with respect to claims 1-9 and 11-24 have been fully considered and are persuasive. The 35 U.S.C §103 Rejection of claims 1-9 and 11-24 has been withdrawn.
11. On 17 November 2004, the Examiner contact Joseph Lutz (Reg. No. 43,765) regarding filing a Terminal Disclaimer to overcome the obviousness Double Patenting Rejection above and making a minor claim amendment to claim 19. Please see the interview summary attached for more details.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

13. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

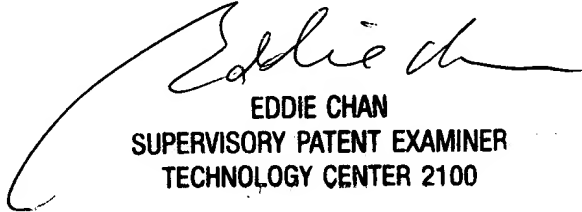
14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

15. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2183

16. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
17 November 2004



EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100